ABSTRACT OF THE DISCLOSURE

An instruction pipeline in a microprocessor includes one or more of the pipelines maintaining a return buffer. Upon detecting a call instruction, a pipeline will push the return address onto its return buffer. The pipeline will then determine if the call instruction was detected by a second pipeline and will send the return address to the second pipeline if the call was not detected by the second pipeline. Upon detecting a return instruction, the pipeline will pop the return address at the top of its return buffer. The return address may then be used in the instruction pipeline. The pipeline will send a request to a third pipeline to fill its return buffer with entries from the third pipeline's return buffer. The pipeline will determine if the return instruction was detected by a second pipeline and will send the return address at the top of its return buffer to the second pipeline if the return was not detected by the second pipeline.